Ansys

Challenges and Opportunities on Thermal Modeling and Simulation for Advanced 3DIC System

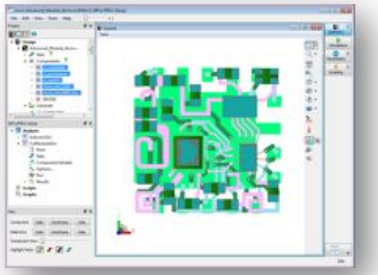
Norman Chang, Ansys Fellow, IEEE Fellow
Chief Technologist of Electronics, Semiconductor, and Optics BU

DAC, 2023

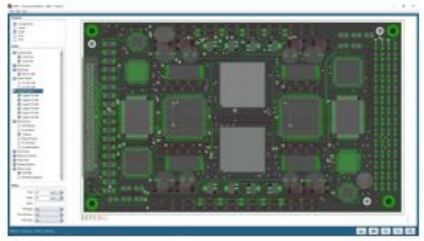
Agenda

- Thermal and reliability challenges on advanced 3DIC system
- Early and layout level thermal/stress analysis much needed for 3DIC
- Thermal throttling simulation required to optimize the placement of increasing number of thermal sensors on 3DIC
- ML-augmented fast static/transient thermal solution demanded for long vectors and multi-mode operations
- Summary

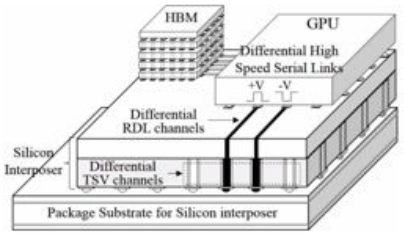
Electronics, Semiconductor and Optics – Thermal/Reliability as Common Challenge



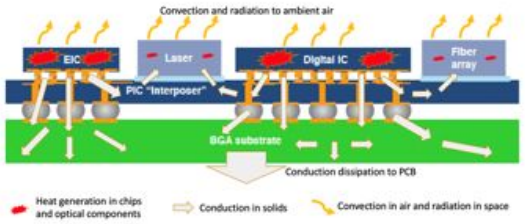
RF, PMIC, AMS



Chip-Package-Board



FinFET and 3D-IC

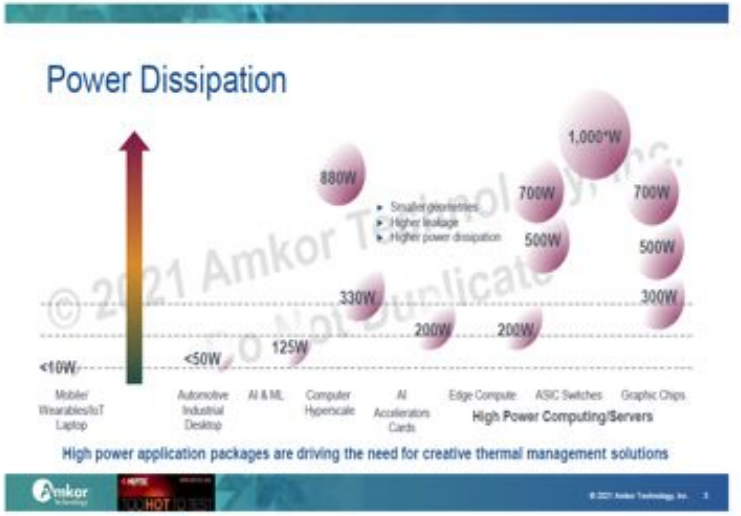


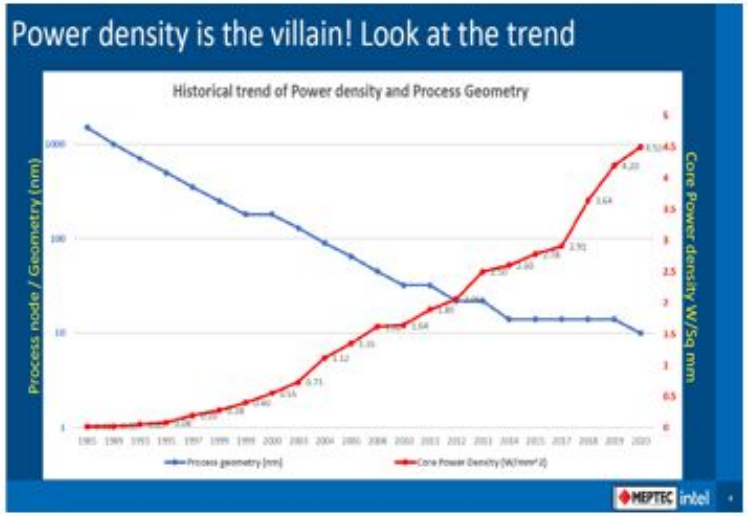
Co-packaged electro-optical

5G/6G and Edge IoT

HPC and Cloud

Automotive, Aerospace and Industrial





Ref : Too Hot to Test, 2021

Multiphysics Solutions for SI/PI/TI/Reliability
(**Electromagnetics, Optics, Thermal**) x (Die, 3D-IC, Package, Board)

Thermal/Reliability challenges for HI 3DIC

- Early and layout level on-chip and package/system thermal/stress analysis
- ESD/EMI/EMC/Rad hard of chip-package-system and on-chip wearout
- High-freq power and signal integrity including TSVs/Interposer
- Co-optimization of package/chip thermal/stress mitigation with ML

3DIC Package Thermal-Mechanical Reliability Mechanisms

Package Mechanical Stresses

Stress-type

Thermo-mechanical Stress

Hygro-mechanical Stress

Electro-Thermo-mechanical Stress

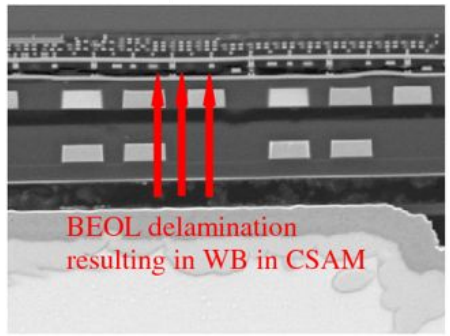
Fail modes

Dielectric cracking
Interfacial cracks

Solder joint fatigue
Cu trace cracking
Package delam. modes

Moisture swelling failure
Vapor pressure induced "Popcorn" cracking

Electromigration
E-T-M trace failures



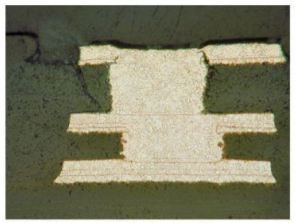
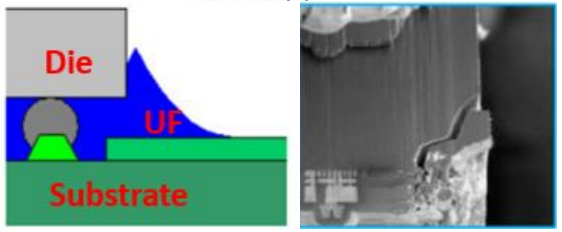
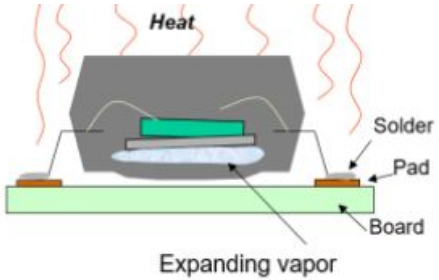
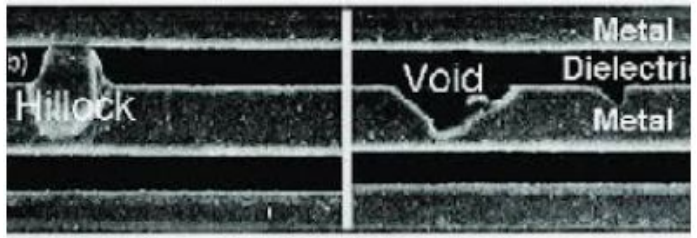
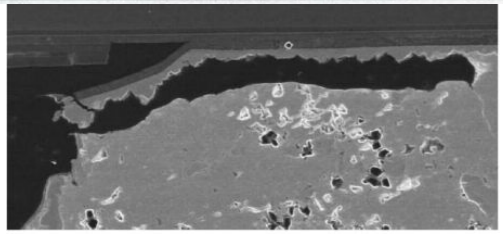


Figure 7: Copper filled microvia with corner crack. Source: Paul Reid [12]

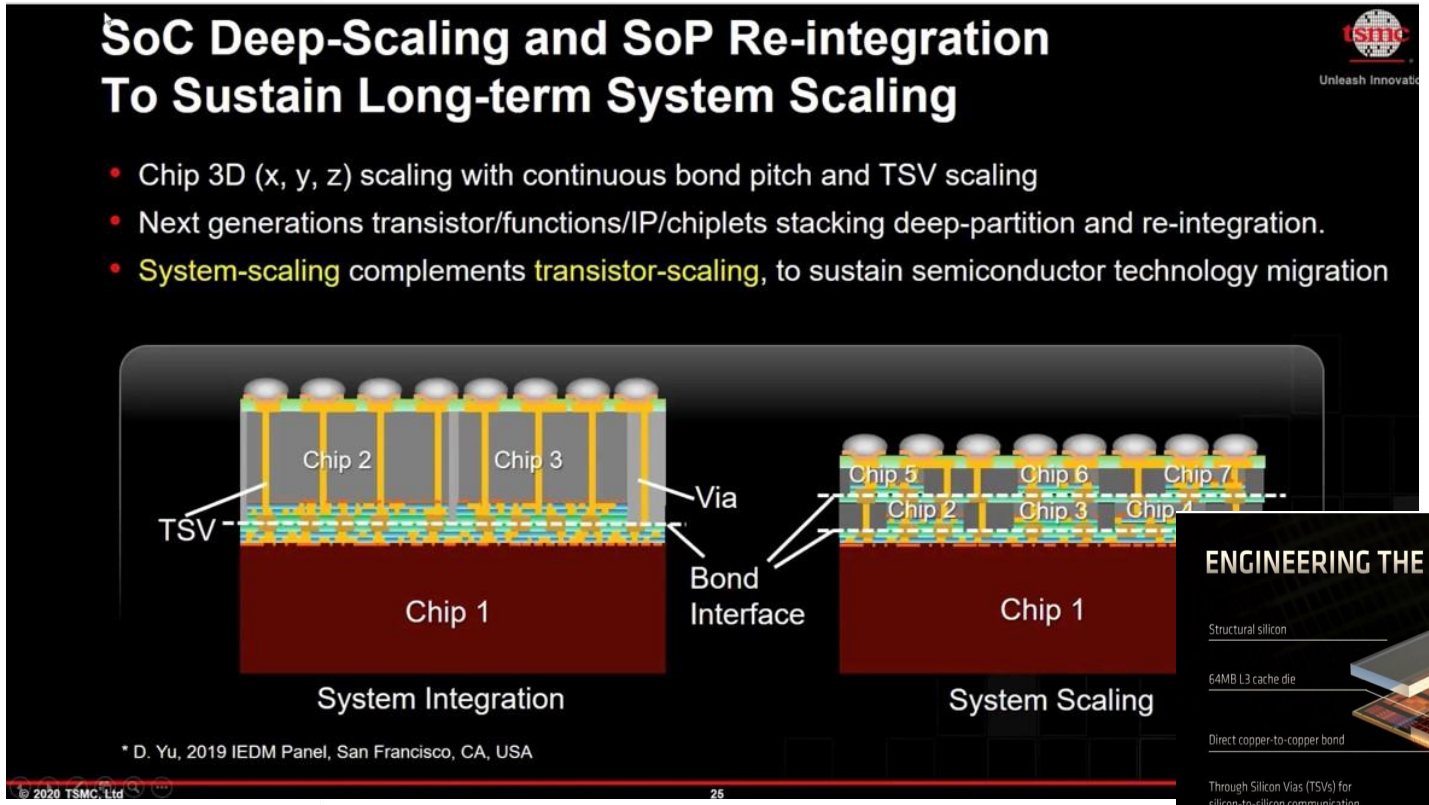




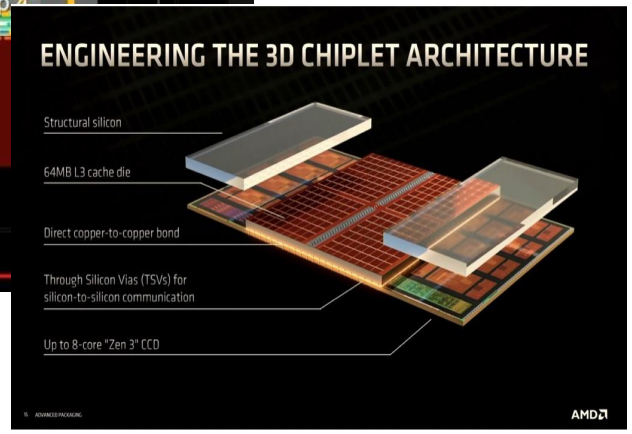




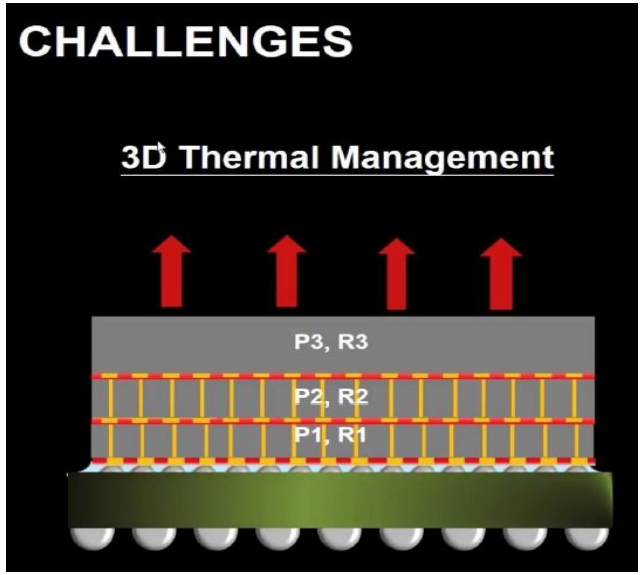
Aggressive System Scaling with 3DIC Requires Thermal/Stress Analysis Solution

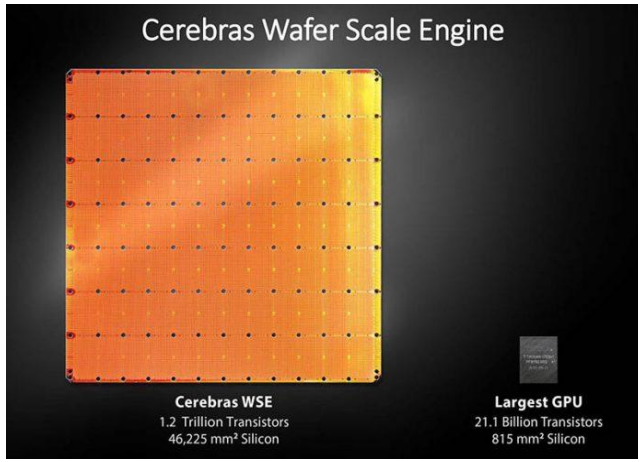


SoIC innovative bump-less bonding



AMD, Hot Chips 2021

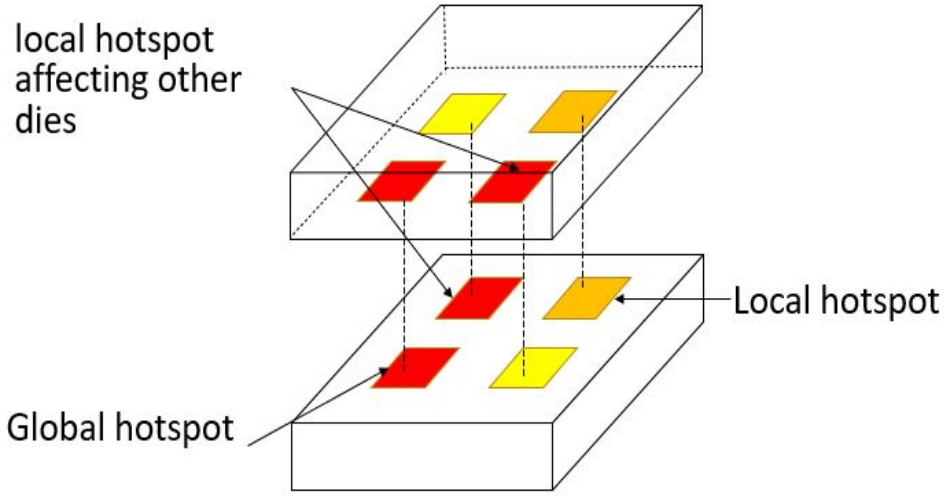


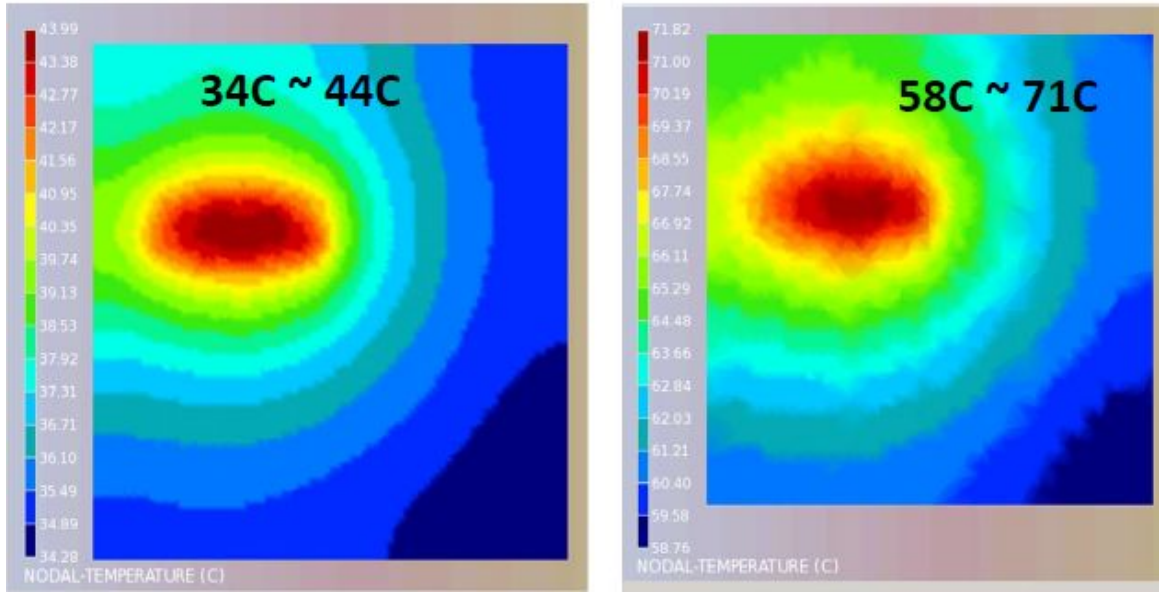


Cerebras, Hot Chips 2021

Doug Yu, TSMC, ECTC keynote speaker, 2020
Focusing on PPAT
(Power/Performance/Area/Temperature)

Challenge for Accurate Multi-Die Thermal Analysis



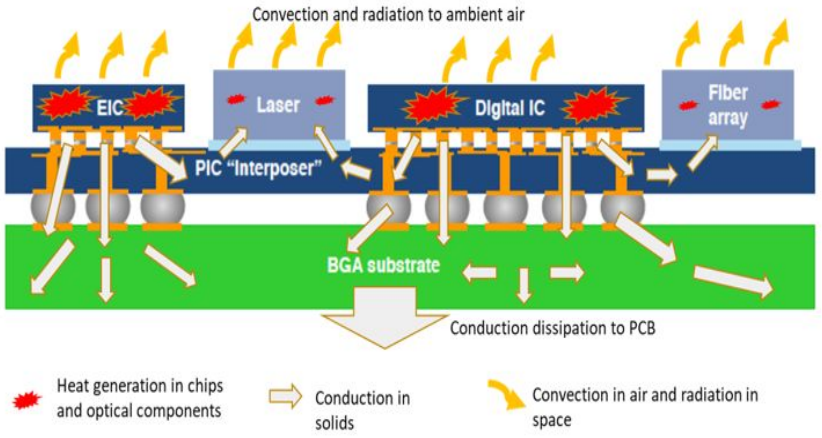


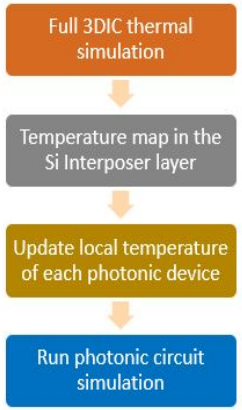
Cross die thermal crosstalk can cause ~20C to ~30C hotspot temperature difference

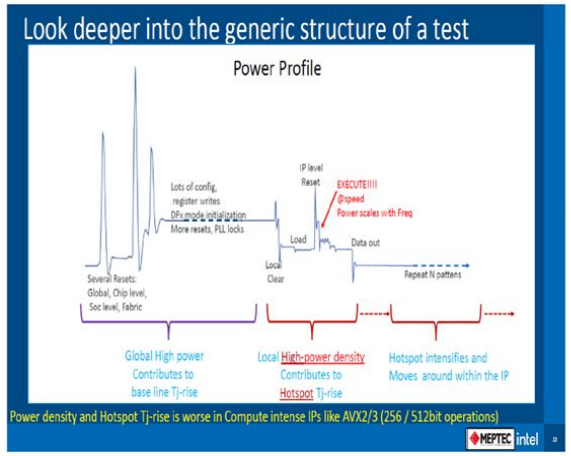
"Effective Hierarchical Thermal Analysis Solution with ML-enabled Technology for 3DIC System", T. Zhang, N. Chang, et al., Ansys, TSMC OIP, 2022.

Emerging Challenges and Opportunities on Thermal Modeling and Simulation for Advanced 3DIC System

Solving for Digital IC and EIC on heat generation
Solving for PIC Package: heat generation, dissipation, and thermal couplings of chips and optical components







- Scan test
  - ✓ Shift in : many chains w/ 100s of MHz, high Cdyn (about 3-10X of real-world application) w/ high total power
  - ✓ Capture @speed : running at GHz of speed for several cycles, high power density / power, severe Vdroop and high Tj-rise at different locations;
    Tj-rise ↓, Fmax ↑, Vmin ↓, Vdroop ↓, Power ↓
- Functional test
  - ✓ Cache load / Structured Based Functional Test, system ported test
  - ✓ Shmoo plot of Fmax, Vmin, Tj-rise, Vdroop, Power
  - ✓ Thousands of test patterns each of 0.5-1msec generating high power density, Tj-rise, and Vdroop
  - ✓ Tj-rise and Vdroop are correlated too due to leakage power exponential dependence of Tj-rise

Ref : Too Hot to Test workshop, Intel, 2021, https://youtu.be/0gPSbZqbXUg

Challenges and opportunities on thermal modeling and simulation for advanced 3DIC systems:

- Performing fine-grained static and transient thermal analysis on large 3DIC designs is required and demand adaptive meshing or machine-learning technology to overcome the limitation using traditional CFD/FEA based solvers.
- Architecture-level thermal and thermal-induced stress analysis are required due to the thermal coupling from cross-die horizontally and vertically with transient-based power profile among chiplets in 3DIC.
- Heterogeneous Integration 3DICs may consist of analog/mixed-signal and digital designs which have very different thermal and stress requirements that need to be co-optimized among chiplets and package in 3DIC.
- For Silicon Photonics 3DICs, accurate thermal gradient analysis is required for the co-optimization of 3DIC package and required thermal heater for PIC design.
- Testing of large 3DIC consisting of CPU/GPUs, etc. presents a major challenge due to multiple localized thermal hotspots and dynamic voltage drop affecting yield. Co-optimization of test techniques and localized thermal hotspots and Vdroop on 3DIC should be considered.

Agenda

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Vision on PI/TI/Reliability Simulation for Advanced 3DIC System

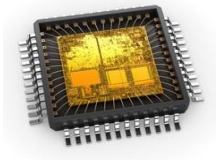
Anticipate Physical Integrity Challenges

New ASIC

- Architecture Design — Spec
- Functional & Logic Design — RTL
- Schematic / Circuit Design — Netlist
- Physical Design — P&R
- Physical Verification — SignOff
- Fab / Foundry / Packaging
- Testing & Certification

/Ansys /Ansys

Production



« Shift **UP** »

« *Shift Left* »

Designers wish to have earlier visibility on the effectiveness of power/thermal/stress integrity

Floorplanning — PG Grid — Placement — CTS — Routing & Timing — SignOff

- Step 1 • Architecture Level PI/Thermal/Stress What-if Flow
- Step 2 • RTL/Gate/CPS PI/Thermal/Stress What-if Flow
- Step 3 • Handling large 3DIC static/transient thermal
- Step 4 • Solving exacerbated CPS/Chip-level reliability issues

Simulation Explorations
Define limits with Physics

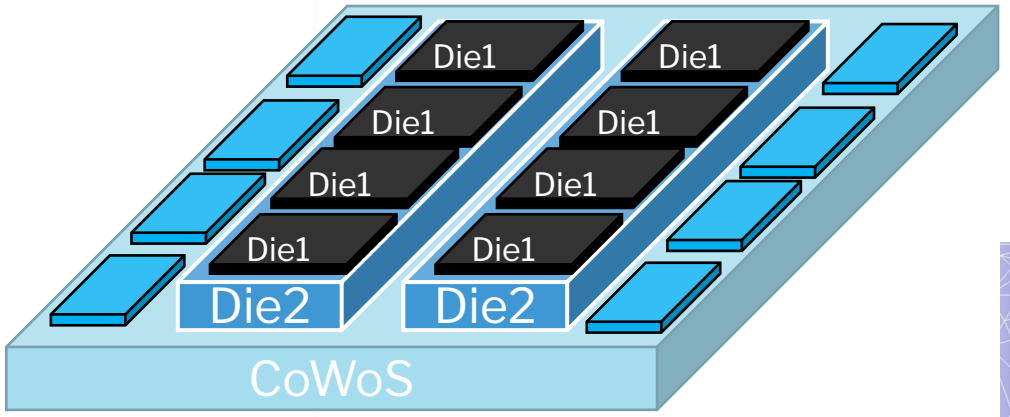
Validation
Confirm Layout with Physics

Qualification
Calibrate the Models

High-Capacity Static Thermal Flow Needed for Large 3DIC

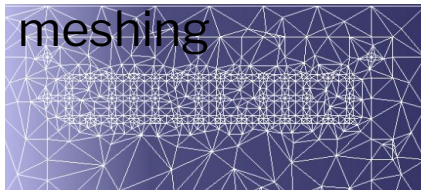
Driving applications: HPC / AI / 5G

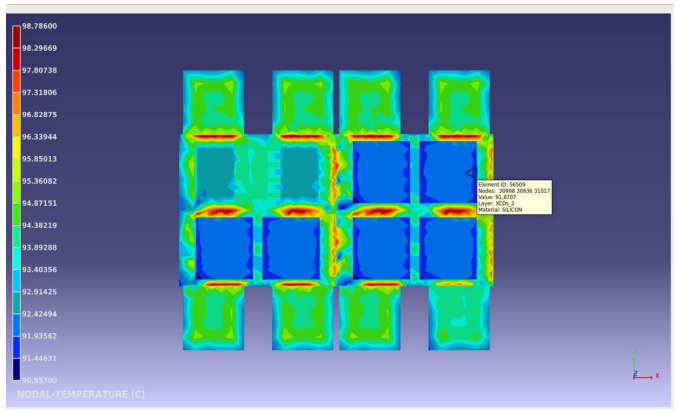
- ✔ Hierarchical CTM stitching technique to assemble the thermal model to handle heterogenous 3D-IC system
- ✔ **Intelligent Adaptive Meshing** can be applied to finish the hierarchical thermal simulation in hours and continue to innovate on fast and accurate hierarchical thermal simulation
- ✔ 3D-IC junction Tmax optimization with HTC applied on the package surface and heat spreader components included.



3D-IC system with CoWoS package

Region-based adaptative meshing

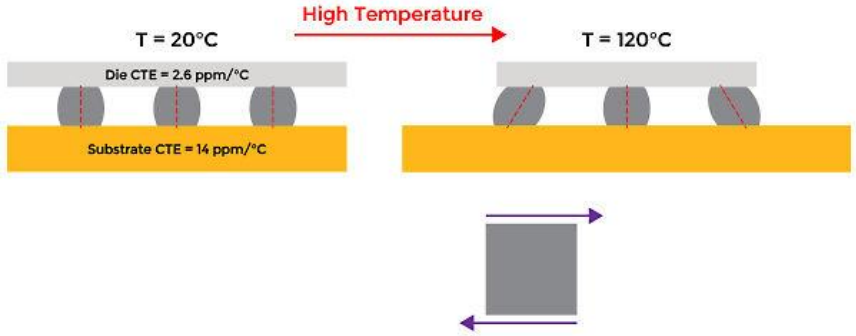




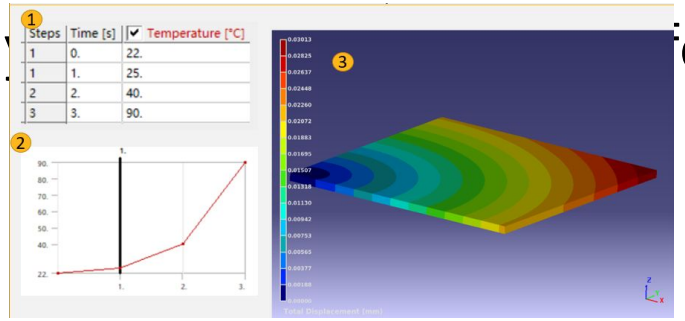
Thermal result for large 3DIC

Thermal-Induced Stress Simulation Methodology

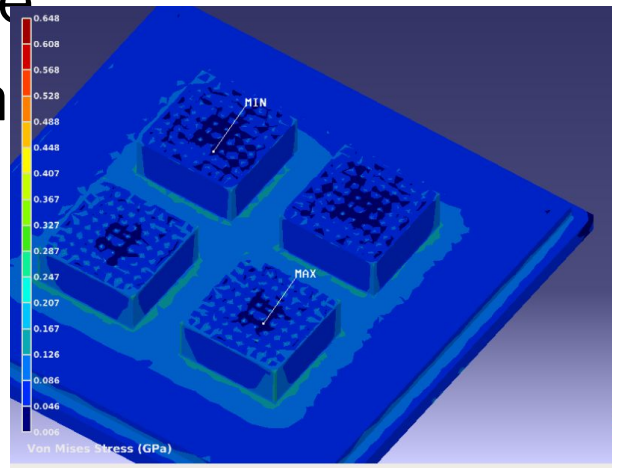
- Mechanical stress caused by change of temperature of a material
  - Thermal expansion during assembly or in operation
  - Thermal cycling in operation with different modes impact on strain/stress
  - Larger size of 3DIC exacerbates the warpage issue



Coefficient of thermal expansion (CTE) mismatch between two materials causes warpage and displacement

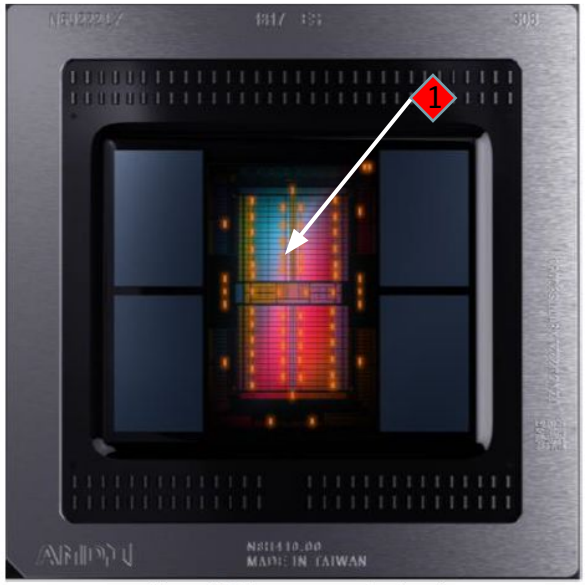


Step-temperature impact on displacement



Von Mises Stress

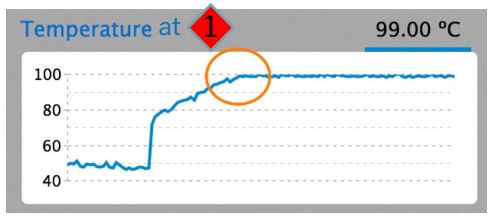
Detailed On-Chip Sensor Based Thermal Throttling Simulation



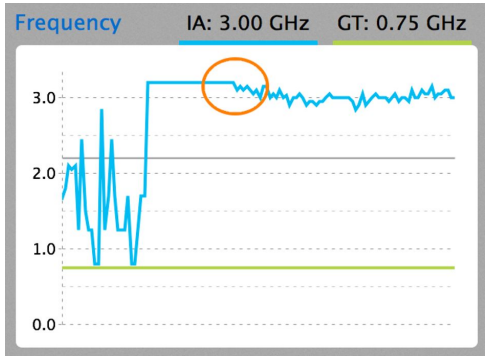
Note: HBM sensors not depicted

64 Sensor locations highlighted on VEGA 20 of Radeon VII card (picture from AMD)

Dynamic Power Mode Selection due to DVFS



If temperature at location 1 reaches the threshold of 100C



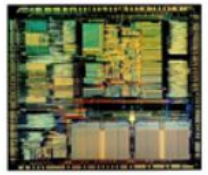
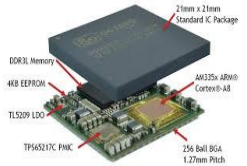
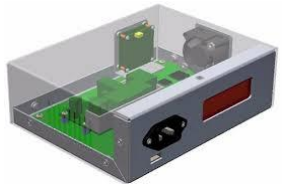
The DVFS control logic lowers the voltage and frequency of the GPU

[Vega 20: Under The Hood - The AMD Radeon VII Review: An Unexpected Shot At The High-End (anandtech.com)]

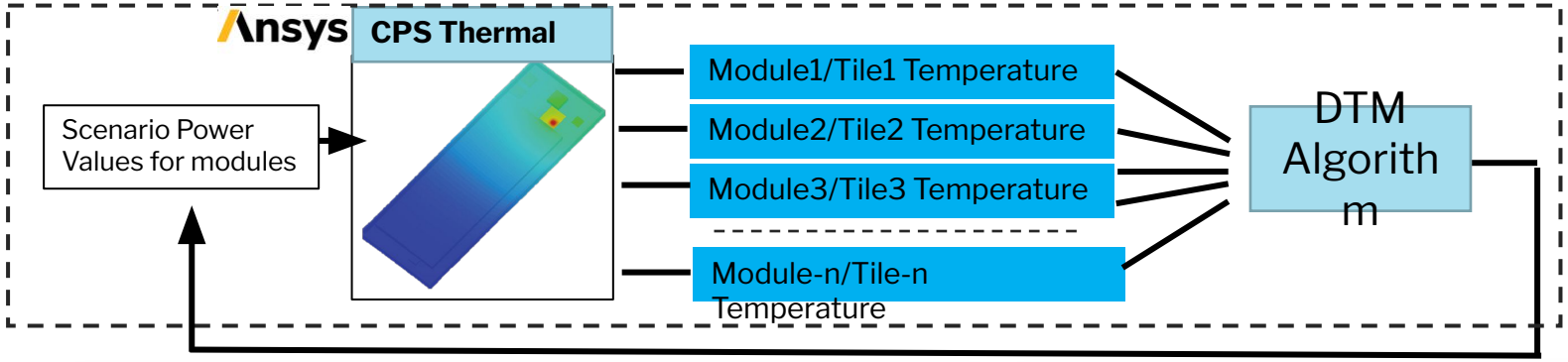
- The trend is that there will be more and more on-chip thermal sensors for DVFS control
- Optimization of on-chip thermal sensor locations are much needed and can be achieved through architecture-level and detailed layout-level thermal simulation

Chip, Package, System Aware Thermal Throttling Simulation
simulating thermal throttling in system

Driving applications: Datacenter / Mobile

IC	Package	PCB	SYSTEM
			

Emulator activity profiling for RTL power
+
Augmented Thermal Simulator
+
RH-SC Electrothermal



However lacking detailed on-chip thermal response

Fast and Accurate Thermal Analysis of Smartphone with Dynamic Power Management using Reduced Order Modelling

Sivasubramani Krishnaswamy, Palkesh Jain, Aniket Kulkarni, Ankit Adhiya
ANSYS Inc., Canonsburg, PA 15317
sivasubramani.krishnaswamy@ansys.com, palkesh@qti.qualcomm.com, aniket.kulkarni@ansys.com, ankit.adhiya@ansys.com

Thermal Sensor Placement based on Meta-Model Enhancing Observability and Controllability

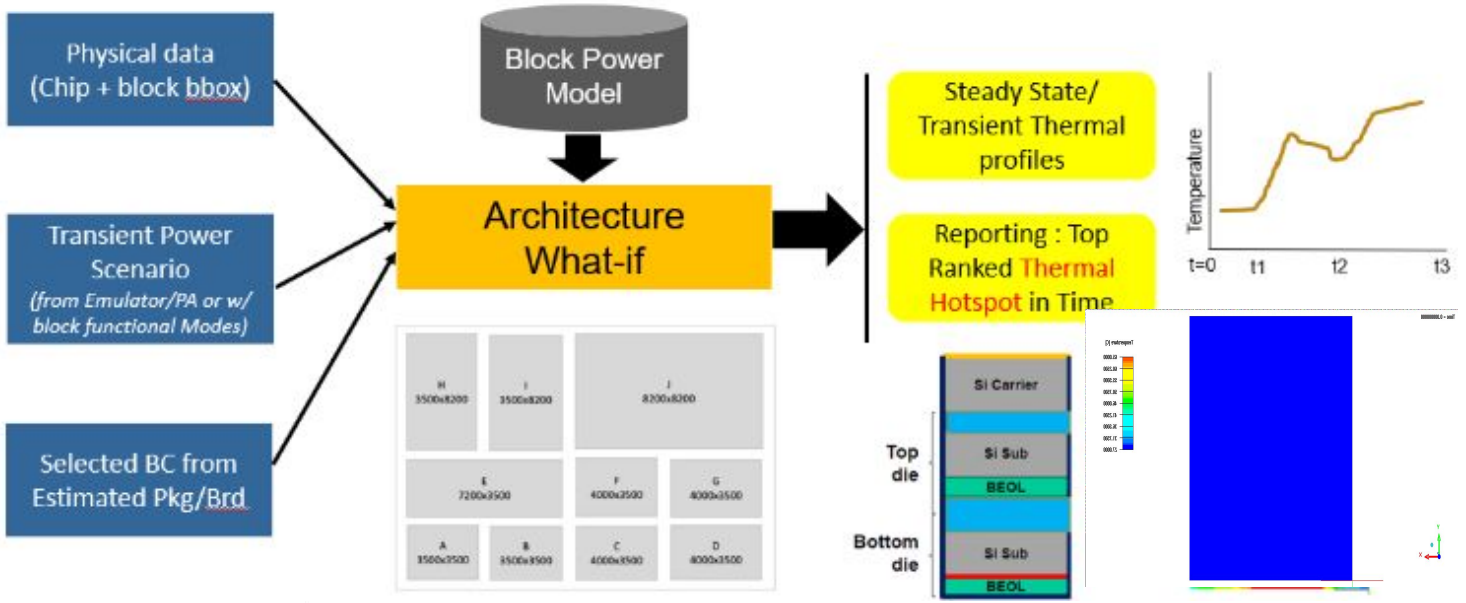
[1]Yunhyeok Im, [1]Wook Kim, [1]Taekeun An, [1]Heeseok Lee, [1]Young-Sang Cho, [1]Jongkyu Yoo, [1]Hoi-Jin Lee, [1]Youngmin Shin
[2]Myunghoon Lee, and [3]Vamsi Krishna Yaddanapudi

[1]Samsung Electronics Co. Ltd
1-1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-do
Korea, 18448

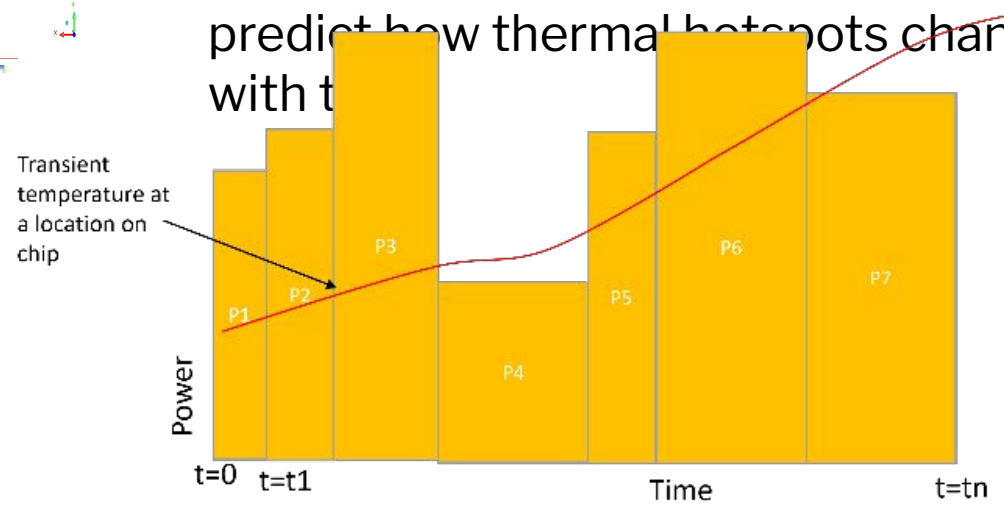
[2]ANSYS Korea LLC, [3]ANSYS Fluent Pvt Ltd

Email: imim@samsung.com

The Need for Fast Static/Transient Thermal Analysis On-chip



- Performance and reliability degradation
  - Aging, EM, IR drops, stress, switching speed, etc.
- Fine grained thermal analysis on large 3DIC designs not possible using traditional FEA/CFD based approaches
- Long sequences of transient power need to be simulated to accurately predict how thermal hotspots change with t



Architecture level fast transient thermal analysis for various optimizations are required.
(i.e. power/DvD/thermal/stress/test/etc.)

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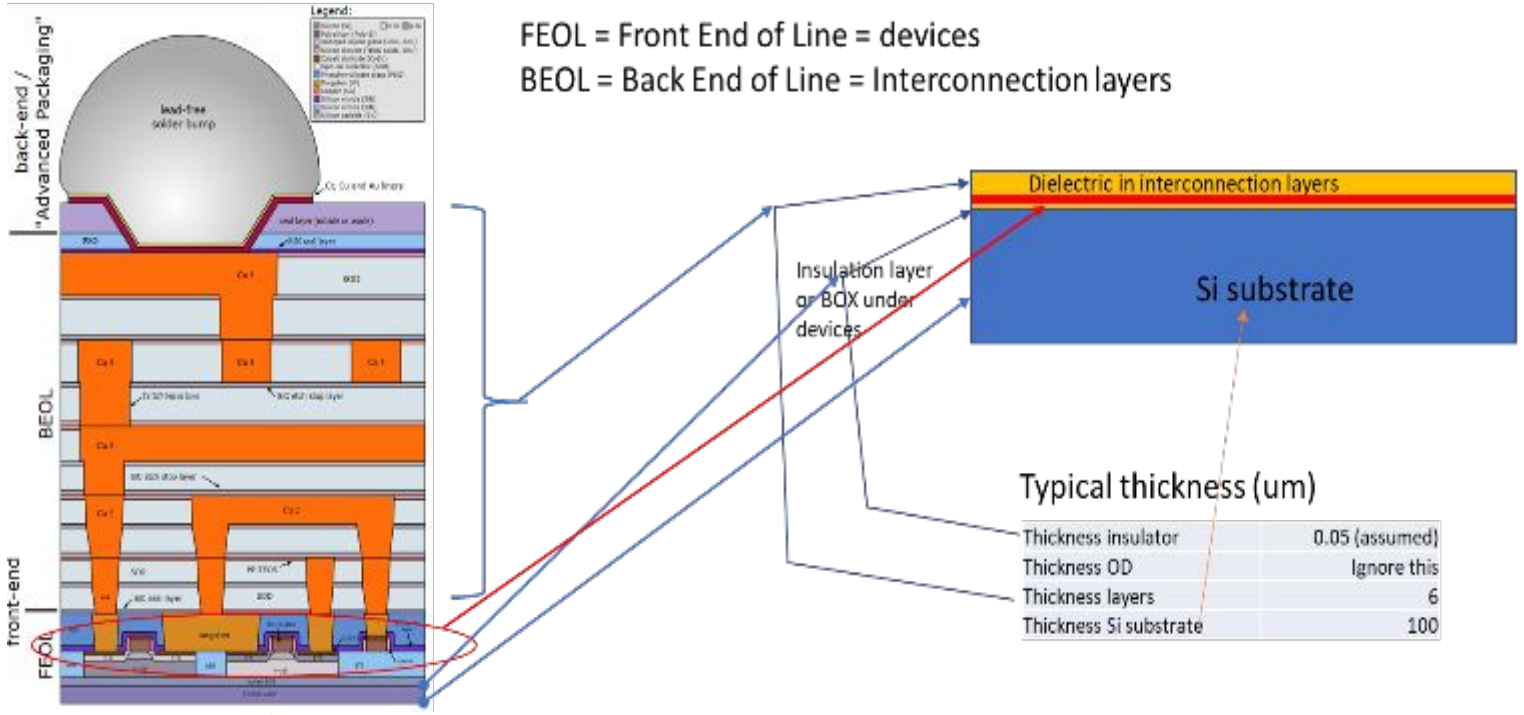
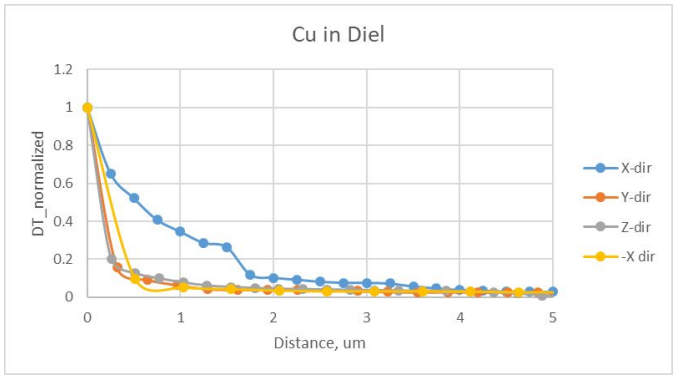
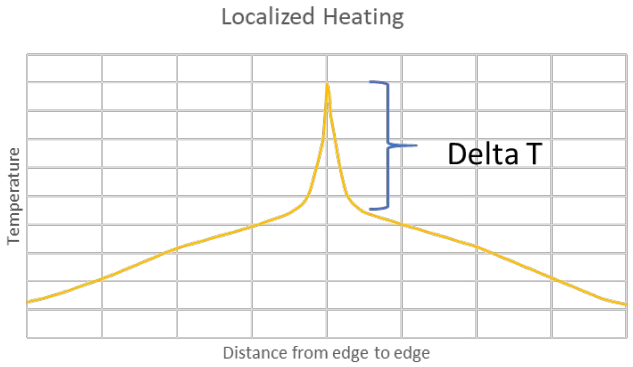
Refined Chip Thermal Modeling of Interconnect/Device Layers



Typical CMOS structure (left) and the thermal global model (right). Power of devices (FEOL) at interface of BEOL and Buried SiO2 (BOX). The local heating characteristics of the near field effect is better captured by the refined chip thermal global model of three layers or more complicated one.

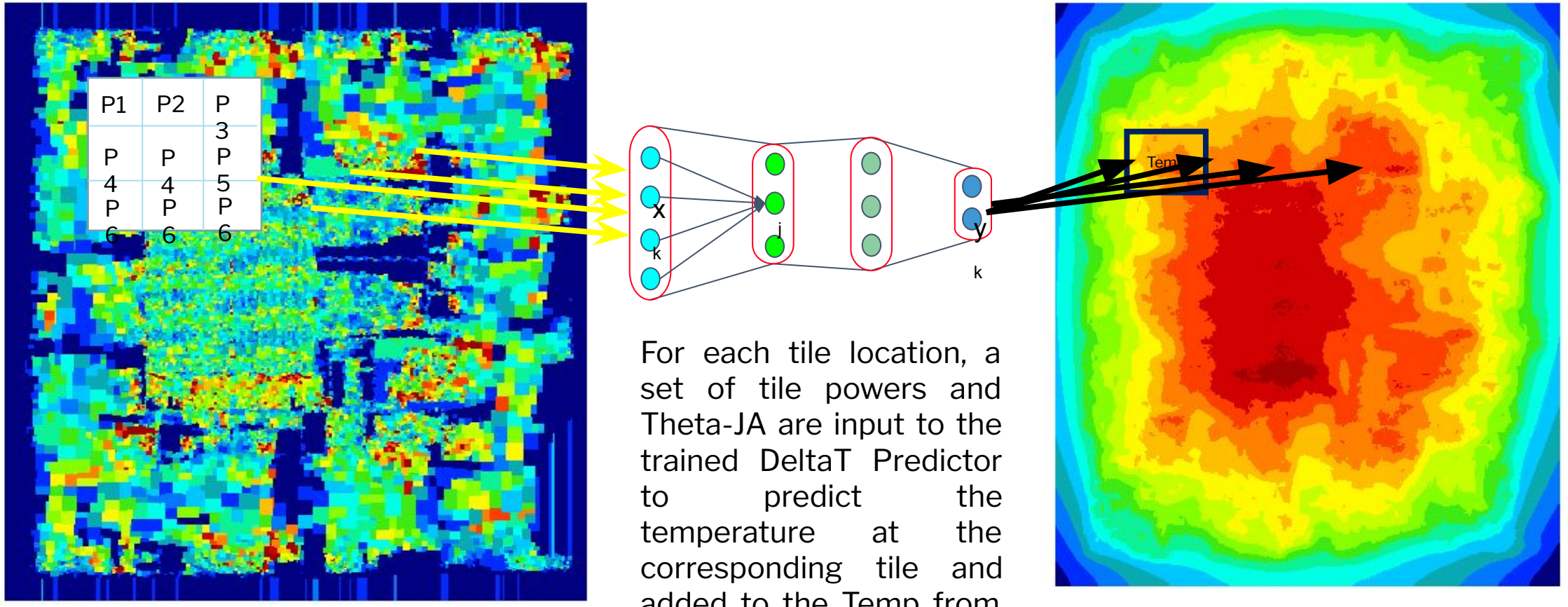


Temperature decay from a heated object in the device or interconnection layers of a deep submicron chip design. (S. Pan, N. Chang, ECTC 2015)



Example of temperature rise due to localized heating on a chip modeled. (J. Wen, S. Pan, N. Chang, et al., IEEE SEMI-THERM, 2020)

Fast ML-Augmented Layout-Based Static Thermal Solver for Horizontal/Vertical Thermal Couplings in 3DIC

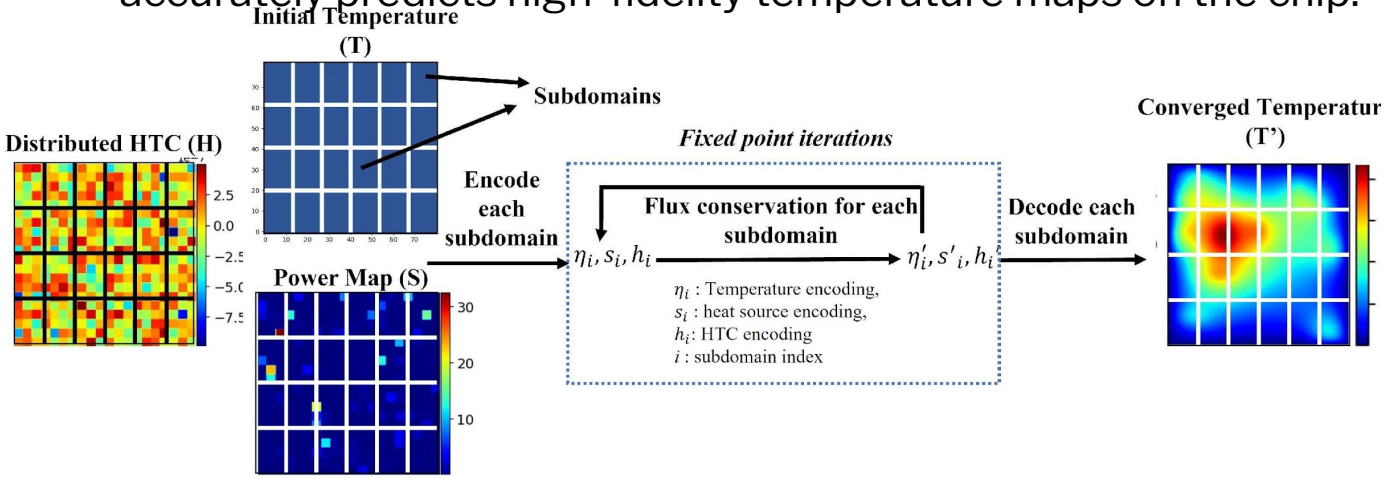


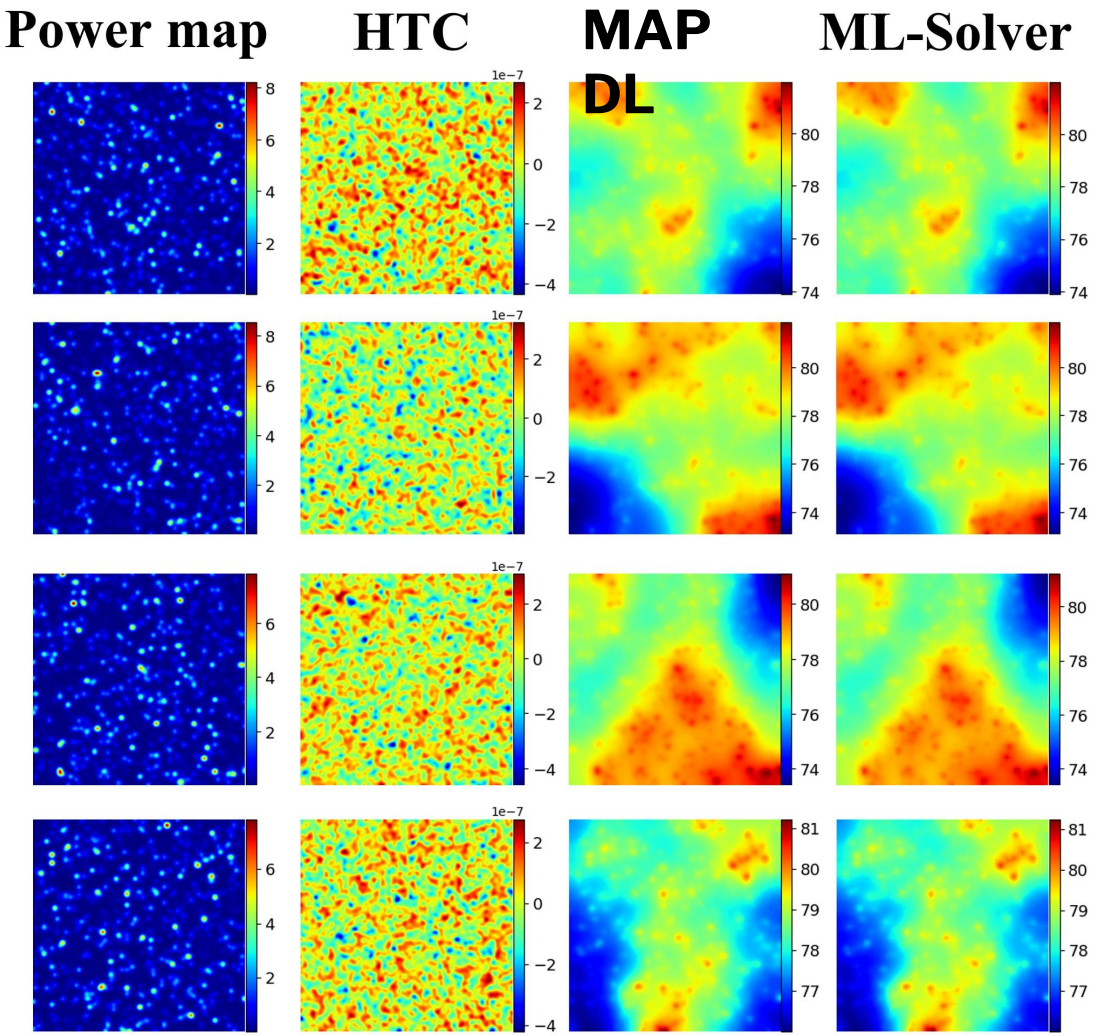
For each tile location, a set of tile powers and Theta-JA are input to the trained DeltaT Predictor to predict the temperature at the corresponding tile and added to the Temp from rough thermal profile

"DNN-based Fast Static Thermal Solver", J. Wen, S. Pan, N. Chang, et al., IEEE SEMI-THERM and Nvidia GTC, 2020
"Effective Hierarchical Thermal Analysis Solution with ML-enabled Technology for 3DIC System", T. Zhang, N. Chang, et al., TSMC OIP, 2022

Machine-learning based Static Thermal Solver with Distributed HTC

- Developed a novel Machine-Learning based Thermal solver to accurately predict chip temperatures for arbitrary power maps and distributed HTC patterns.
- The ML-Solver is inspired from keys ideas of traditional Ansys solvers. It iteratively solves for temperature on discrete subdomains given the power map, HTC and initial temperature. Flux conservation in each iteration is established using pre-trained ML models
- The ML-Solver is about 100x faster than current solvers and accurately predicts high-fidelity temperature maps on the chip.

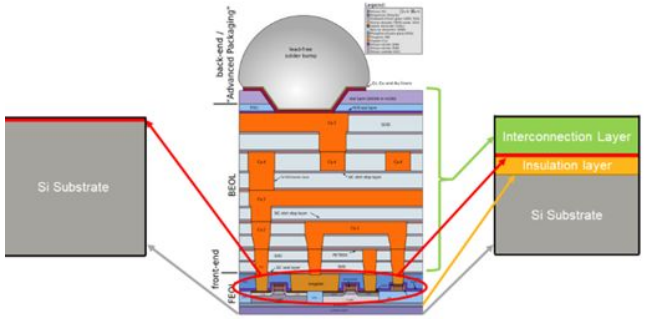




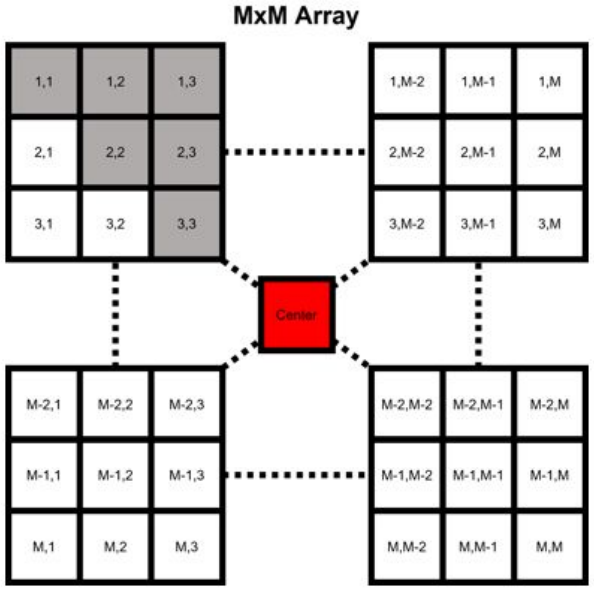
Ranade, R., Haiyang, H., Pathak, J., Kumar, A., Wen, J. & Chang, N. (2022). A Thermal Machine Learning Solver for Chip Simulations. *4th ACM/IEEE Workshop on Machine Learning for CAD*

Fast Transient Thermal Analysis with Decay Surface Model

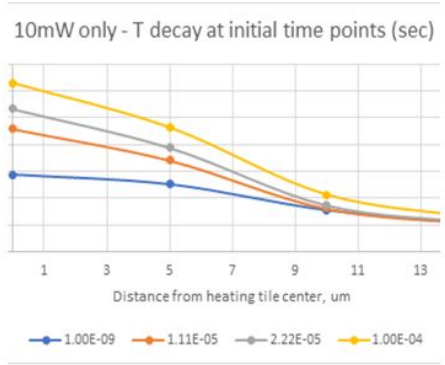
Solution Overview : Fast Transient Thermal Analysis



A 3-layer chip model for transient thermal analysis is used



Transient Decay Surface from Neighboring to Victim Tiles



$$\Delta T_{ij} = f(d_{ij}, t)$$

$$\Delta T_i = \sum_j T_{ij} \quad \forall j \in H$$

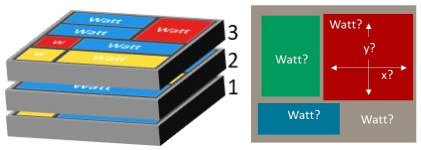
- The term ΔT_{ij} denotes the temperature change at the *ith* location due to *jth* on-chip heat source.
- Linear Time Invariant (LTI) system and therefore the contribution of each of the on-chip heat sources can be linearly combined to generate the total effective transient response at the *ith* location as in equation
- Multi-scale decay surface
  - Local level decay surface to capture the impact of nearby heat sources
  - Intermediate level decay surfaces to capture the impact of intermediate distance heat sources
  - Global decay surface to capture the effect of complete CPS

"ML-based Fast On-Chip Transient Thermal Simulation for Heterogeneous 2.5D/3D IC Designs", A. Kumar, N. Chang, et al., IEEE VLSI-DAT, 2022

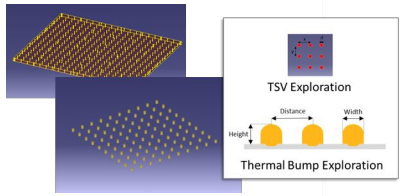
"On-chip Transient Hot Spot Detection with a Multiscale ROM in 3DIC Designs", D. Geb, N. Chang, et al., IEEE ECTC, 2022

ML-based Power & Thermal Design Space Exploration in System Technology Co-optimization (STCO)

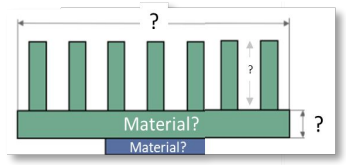
CTM, other power source



Die/pkg/pcb/tsv/bump model



Heatsink, Boundaries model



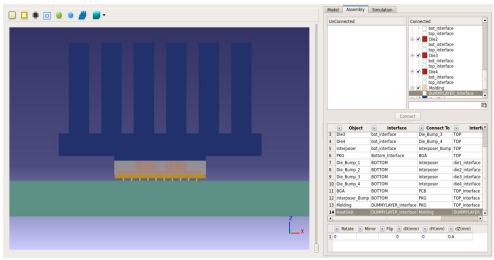
✔ **Bill of Material**
✔ **Architecture**

Exploration module
Power, Heatsink, BC

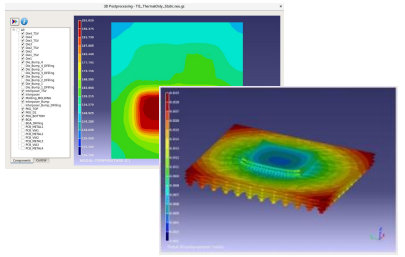
Goals setting
Max T°, Gradient, Warpage…

/**ML Optimizer**

Model Assembly → Static, Transient → Temp contour, Thermal Stress, …



Thermal /Stress Solvers

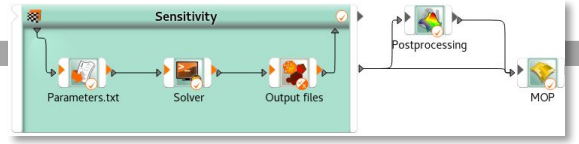


✔ **Performances**
✔ **Cost**

Results Postprocessing
✔ **Warpage**
✔ **T°**$_{Max}$ (EM)
✔ **ΔT°** (Timing)

/**ML Optimizer**

Variable Sweeping



ML-based MetaModel Training

Sensitivity Analysis

Need for “Thermal aware” Architecture Validation with the Help of Machine Learning

Optimization of Mobile Pkg Material Calibration for Thermal Integrity

As-is process/Challenges

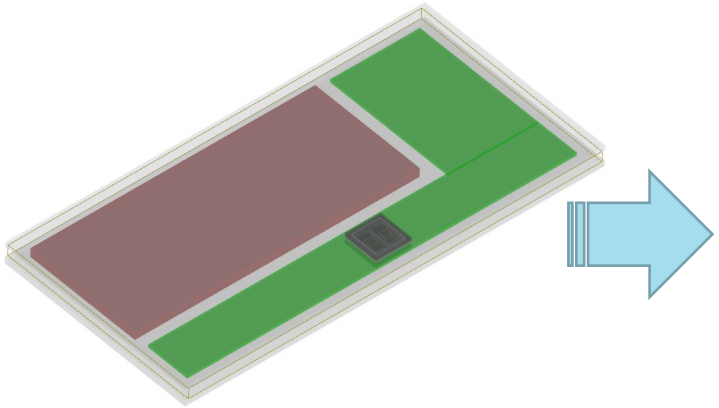
- Sensitivity analysis of thermal material properties of mobile AP
- Fast and Accurate equivalent virtual thermal testing model Simple Model
- Trial & Error approach for fine tuning material Expensive!
- Too many trials (1000+) need to be performed for 10+ parameters
- Challenges:
  - Significant manual effort for 1000+ trials
  - Accurate simple model for transient thermal analysis

Ansys Value Stream

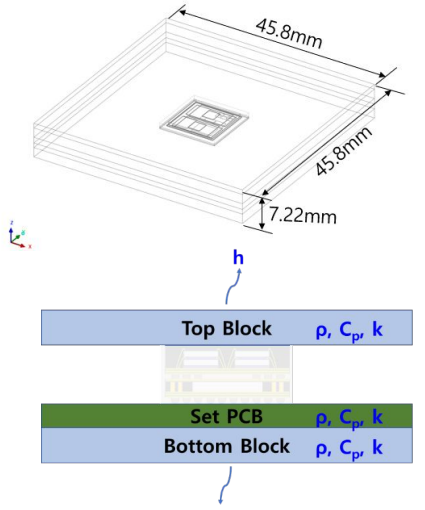
- Robust workflow integration and optimization with optiSLang-AEDT Icepak
- Reduced input BC conditions and material properties (h,K,CP and Den)
- Sensitivity analysis with thermal material parameter of components.

Outcome

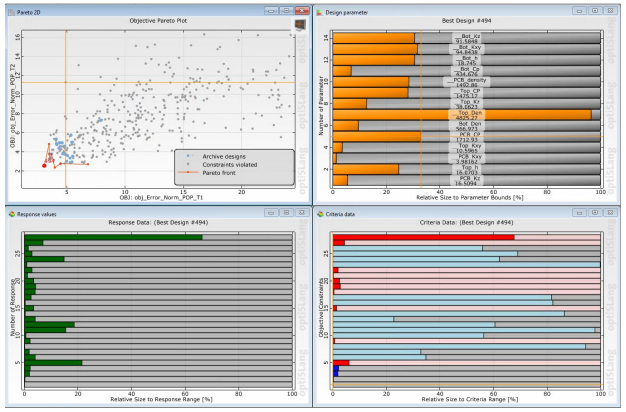
- Extract optimized equivalent properties of Simple model that is well matched with reference data
- Automatic DOE reduction to reduce the overall time for optimization.
- Reduced time for optimization and increased accuracy
  - 2~4 Weeks 4~5 Days

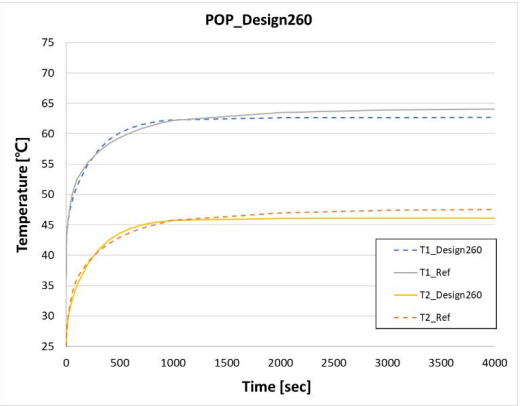


Full set model of smartphone



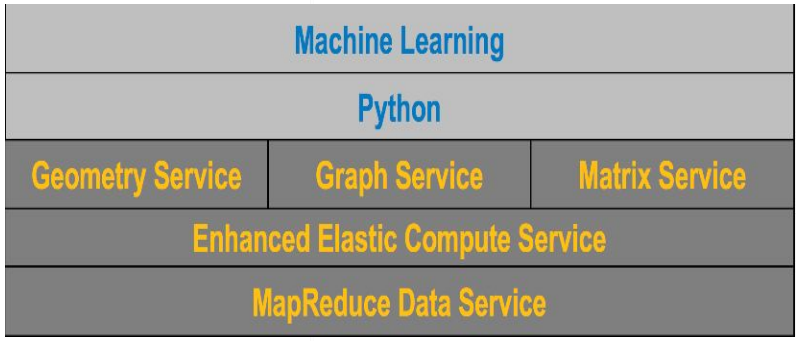
Simple model with equivalen thermal material property



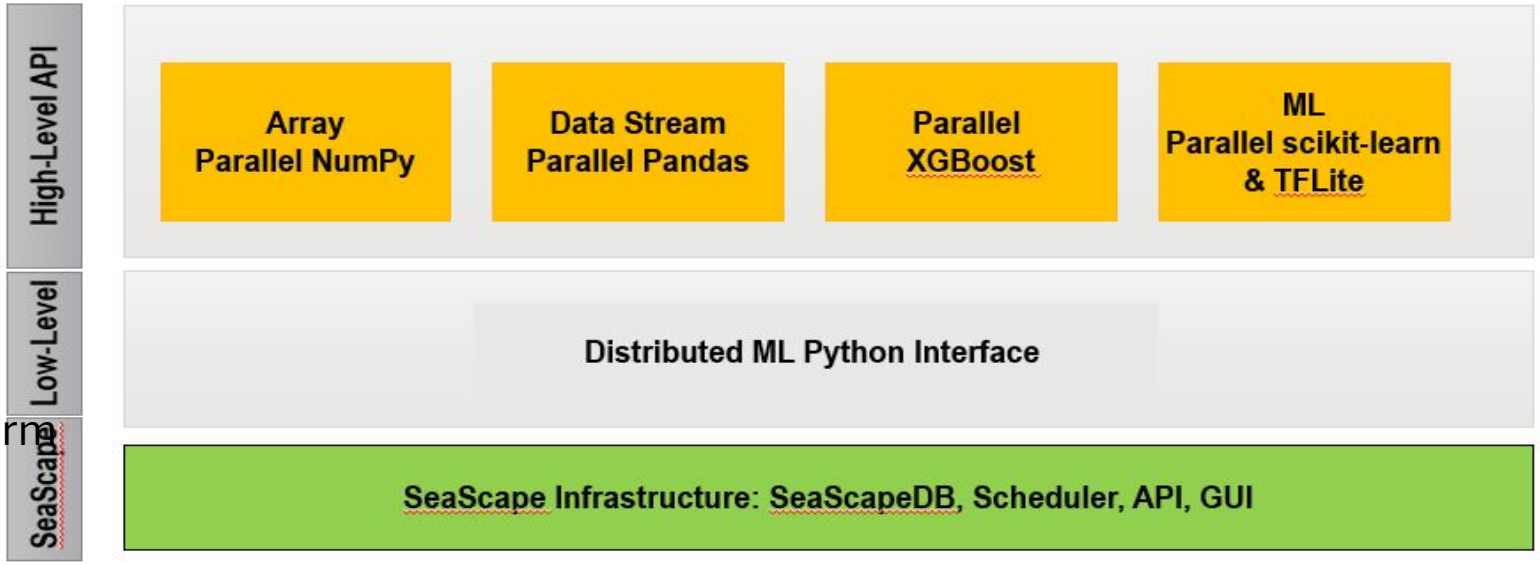


"Thermal Model Simplification of Mobile Device with Adaptive Metalmodel of Optimal Prognosis (AMOP)", V. Krishna, et al., iTherm, 2022

Thermal Multi-physics Solving Augmented by Distributed ML Framework



SeaScape Distributed Computational Platform



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2. "A Thermal Machine Learning Solver for Chip Simulation", R. Ranade, H. He, J. Pathak, N. Chang, A. Kumar, J. Wen, IEEE MLCAD, 2022
3. "ML-based Fast On-chip Transient Thermal Simulation for Heterogeneous 2.5D/3D IC Designs", N. Chang, A. Kumar, J. Wen, H. He, S. Pan, D. Geb, W. Xia, S. Asgari, M. Abarham, Q. Li, Y. Li, Z. Feng, IEEE VLSI-DAT, 2022
4. "On-chip Transient Hot Spot Detection with a Multiscale ROM in 3DIC Designs", D. Geb, S. Asgari, A. Kumar, J. Wen, N. Chang, S. Pan, M. Abarham, H. He, V. Gandhi, IEEE ECTC, 2022
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9. Haiyang He and Jay Pathak. 2020. An unsupervised learning approach to solving heat equations on chip based on auto encoder and image gradient. arXiv preprint arXiv:2007.09684 (2020).
10. "DNN-based Fast Static On-chip Thermal Solver", J. Wen, S. Pan, N. Chang, W. Chuang, W. Xia, Deqi Zhu, A. Kumar, E. Yang, K. Srinivasan, Y. Li, IEEE SEMI-THERM, 2020.

Summary

- Key thermal challenges for 3DIC are outlined as the following
  - Thermal dissipation mechanism needs to be carefully designed since it is harder for hotspot mitigation in the middle of stacked dies
  - Peak static/transient temperatures need to be considered when analyzing die-to-die thermal coupling
  - Early co-optimization of thermal and power partitioning among chips is a must
  - Thermal-induced stress for large 3DIC designs needs to be considered

- Due to increased integration of chiplets in 3DIC designs, the demand for fast static/transient thermal simulation is increasing. Designers must consider an increasing number of workloads and scenarios across the varying IPs and chips for system booting, benchmarking, and wafer/product testing optimizations

Acknowledgement

- Thanks to Akhilesh, Jimin, David, Mehdi, Saeed, Haiyang, Rishi, Wenbo, Prakash, Chris, Lang, Jerome, Preeti, Hua, Jay, and Ying for many discussions on thermal/stress simulation

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- Also thanks to D. Liang and Youn of HPE for thermal simulation collaboration in 3DIC SiPh system